AMENDMENT TO CLAIMS

In the Claims

Please **AMEND** claims 4, 6, 11, 13-18 as follows.

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Original) A method of enhancing stress in a semiconductor device having a gate stack disposed on a substrate, comprising:

depositing a nitride film along a surface of the substrate and the gate stack,

wherein the nitride film is thicker over a surface of the substrate and thinner over a portion of the gate stack.

2. (Original) The method of claim 1, further comprising forming a spacer adjacent only a lower portion of the gate stack.

3. (Original) The method of claim 2, wherein forming the spacer comprises reducing a size of the spacer.

4. (Currently Amended) The method of claim 3, wherein the reducing of the size of the spacer comprises reactive ion etching.

5. (Original) The method of claim 1, wherein the nitride film is a non-conformal nitride film.

6. (Currently Amended) The method of claim 1, wherein the depositing of the nitride film comprises a plasma enhanced vapor deposition process.

7. (Original) The method of claim 1, wherein the deposition of the nitride film provides enhanced stress within a transistor channel.

8. (Original) A method of enhancing stress in a semiconductor device, comprising:

depositing a layer of nitride film over a gate stack and a surface of a substrate; and

removing the nitride film on the gate stack to provide enhanced stress in a transistor channel under the gate stack.

9. (Original) The method of claim 8, further comprising depositing a resist material on a surface of the nitride film over the substrate while leaving a surface of the nitride film proximate an upper portion of the gate stack exposed.

10. (Original) The method of claim 9, further comprising removing an upper portion of the gate stack and the nitride film disposed thereon.

11. (Currently Amended) The method of claim 9, wherein the depositing of the resist material comprises depositing one of a spin-on material, an anti-reflection coating, an oxide film, and a low k material.

12. (Original) The method of claim 11, further comprising forming spacers at a lower portion of the sidewalls of the gate stack.

13. (Currently Amended) The method of claim ~~11~~ 12, wherein the forming of the spacers includes forming the spacers along substantially all of the sidewall and etching the spacers to form spacers at the lower portion of the sidewalls.

14. (Currently Amended) The method of claim ~~11~~ 9, wherein the depositing ~~a~~ of the resist material comprises depositing at least one of an oxide layer or a borophosphorosilicate glass on low spots and leaving high spots exposed.

15. (Currently Amended) The method of claim 10, wherein the removing ~~a~~ of the upper portion of the gate stack and the nitride film disposed thereon comprises reactive ion etching.

16. (Currently Amended) The method of claim 10, wherein the removing ~~a~~ of the upper portion of the gate stack and the nitride film disposed thereon comprises chemical mechanical polishing.

17. (Currently Amended) ~~The method of claim 8, further comprising~~ A method of enhancing stress in a semiconductor device, comprising:

depositing a layer of nitride film over a gate stack and a surface of a substrate;

removing the nitride film on the gate stack to provide enhanced stress in a transistor channel under the gate stack;

forming a spacer adjacent a sidewall of the gate stack; and

etching upper portions of the spacer to form sidewalls only at a lower portion of the ~~sidewalls~~ gate stack.

18. (Currently Amended) The method of claim 8, wherein ~~the~~ a gate is about 60 nm wide, a spacer is about 50 nm wide, and the nitride film provides a stress of about 2.0 GPa, the enhanced stress in the transistor channel is greater than approximately 4.5×10^9 dynes/cm^2 at about 5 nm below a gate oxide.

19. (Original) The method of claim 8, wherein for a semiconductor device having a gate about 60 nm wide, a spacer about 50 nm wide, and a nitride film stress of about 2.0 GPa, the enhanced stress in the transistor channel is greater than approximately 5.5×10^9 dynes/cm^2 at about 5 nm below a gate oxide.

Claims 20-24 (Cancelled).